AMC13 firmware for G-2

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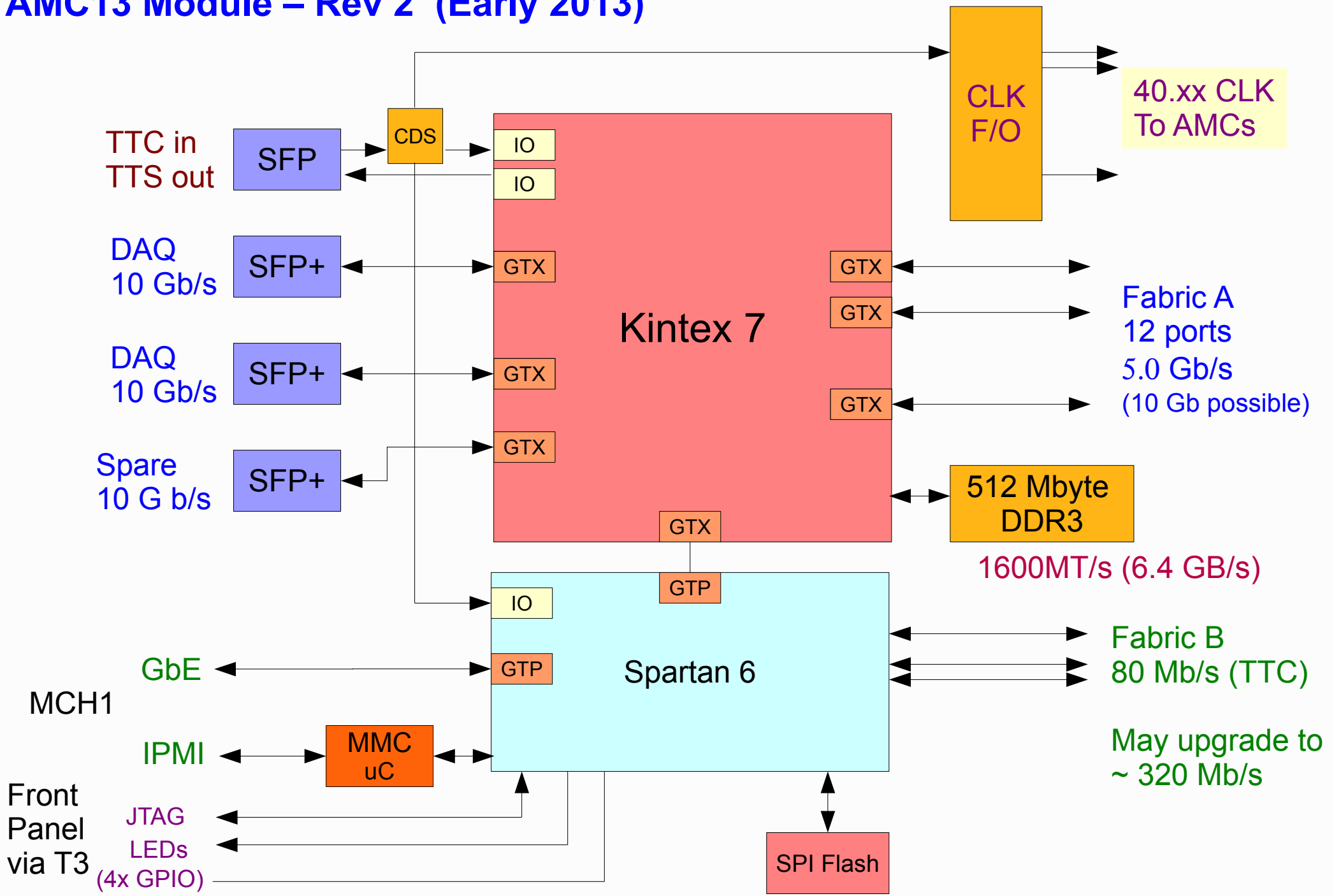
AMC13 Status

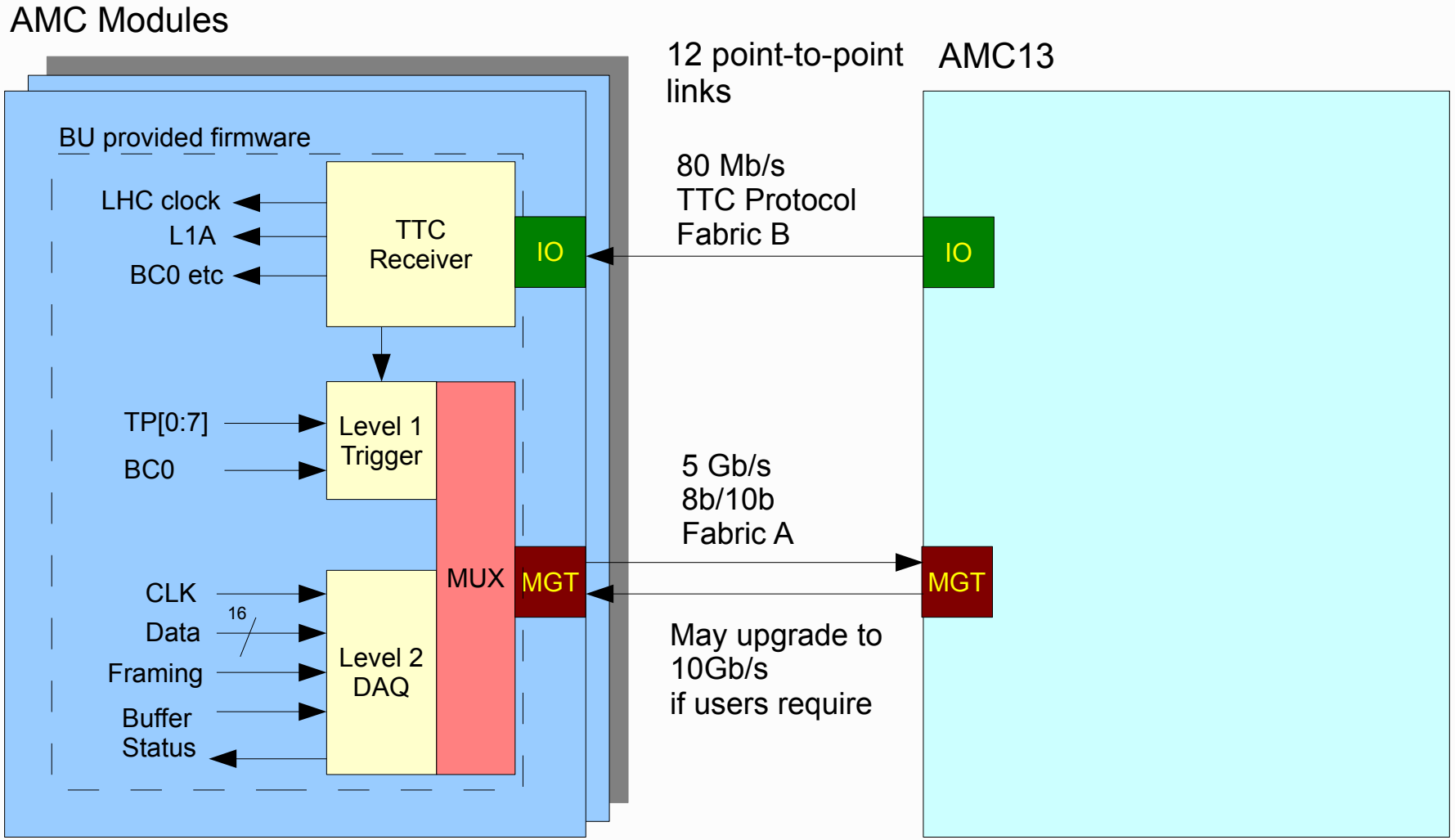
- AMC13XG (10Gb/s) design revision completed
  - Preliminary gerbers submitted to fab for review
- Estimate prototypes by Mid-February 2013
- CMS firmware not suitable for g-2 readout (but could possibly be used for interim testing)
- Custom g-2 firmware is a 1-2 man-month effort (subject of today's meeting)

AMC13 Module – Rev 2 (Early 2013)



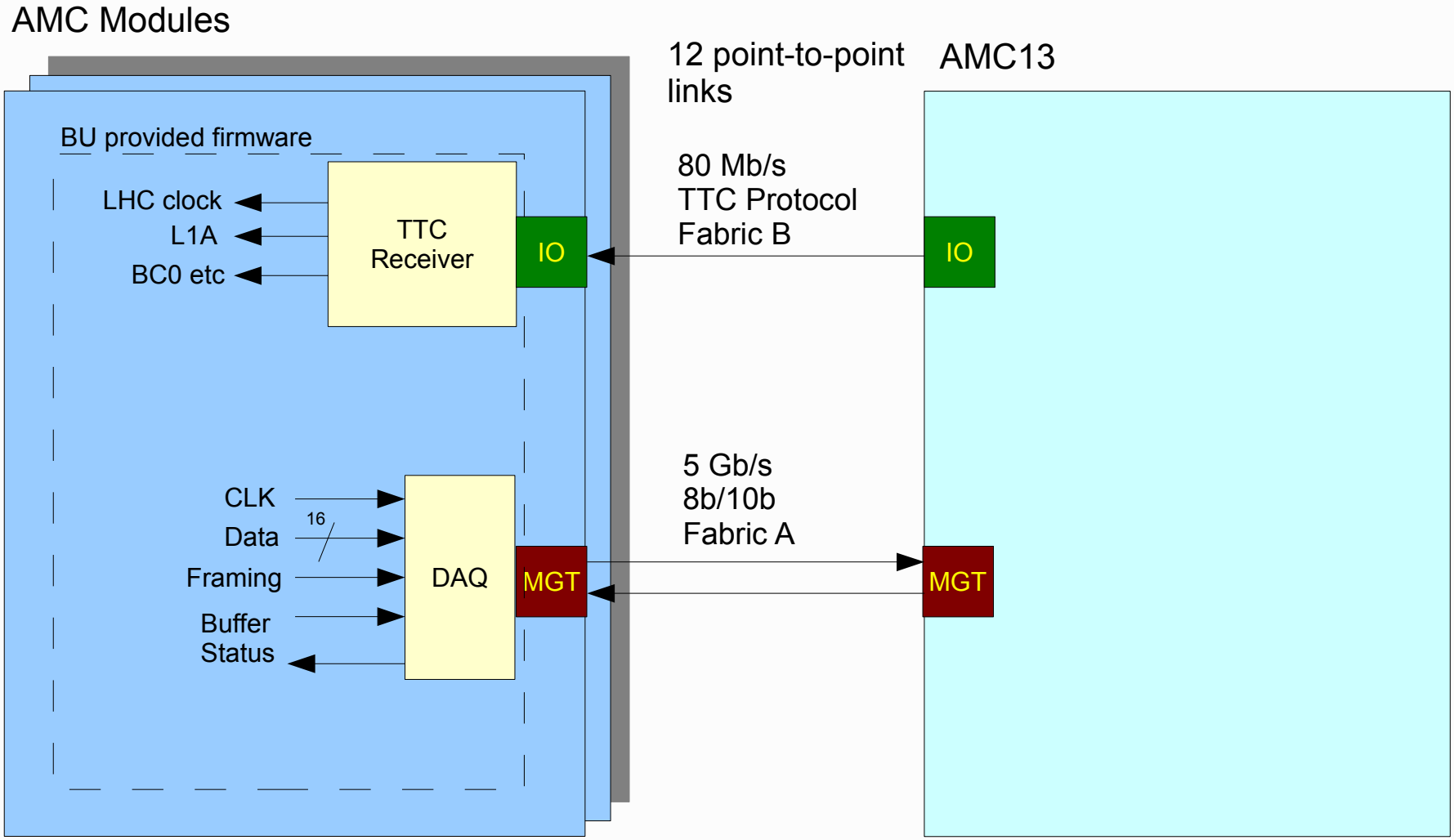
AMC13 Backplane Links - CMS

Backplane Link for TTC / DAQ from AMC to AMC13
Reference design including both ends of link provided



AMC13 Backplane Links - g-2

Proposed modification for G-2
(eliminate trigger path and associated overhead)



Triggering / Fast Controls

- AMC13 distributes an L1A (trigger)
  It has built-in capability to generate test L1A
- Each AMC must send one block per L1A, which is built into an “event” and sent to DAQ.
- This is fine if we redefine L1A = “spill” for G-2
- We may need other “fast” signals defined (can use TTC broadcast commands)
  - These should be defined soon

Data Format AMC→AMC13

Word	FM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	Reserved								EvN[7:0]							
1	0	EvN[23:8]															
2	0	1	AMC Status Bits														
3	0	OrN[4:0]					AMC ID (unique module ID)										
4	0	Format Version					BcN[11:0]										
5	0	Reserved															
6	0	Optional additional header word															
7	0	Optional additional header word															
…	0	Payload															
	0																
	0																
n-2	0	CRC16															
n-1	0	EvN[7:0] for checking								Reserved							

Notes:

- Words 0-4 and last 2 should be formatted as above. Don't use words 5..7.
- Total number of words must be even (pad payload if necessary)
- EvN ("event number") must reset to 1 and increment once per spill
- BcN and OrN are bunch and orbit count for LHC and could be redefined / ignored (They are checked for match between all AMCs and AMC13)
- Payload currently limited to 4096 bytes. Can be expanded, but we should decide once on a size for G-2 as it is difficult to make flexible

Hypothetical G-2 WFD Payload

Header	Card header			
Channel 0	Rec Len [15:0]			
	Spare	P=0	Channel ID	Rec Len[19:16]
	Spare	Sample 0		
	Spare	Sample 1		
		Sample 2		
	Spare	Sample n		
Channel 1	Rec Len [15:0]			
	Spare	P=1	Channel ID	Rec Len[19:16]
	Sample 1 [3:0]	Sample 0 [11:0]		
	Sample 2 [7:0]	Sample 1 [11:4]		
	Sample 3 [11:0]			Sample 2 [11:8]
	Sample 5 [3:0]	Sample 4 [11:0]		
	Sample 6 [7:0]	Sample 5 [11:4]		
	Sample 7 [11:0]			Sample 6 [11:8]
	Channels 2..4			
Trailer	Card Trailer			

Payload size (5 channels)	700us spill	1ms spill
With P=0 (word-aligned):	1.75E6 16 bit words	2.5E6
With P=1 (packed):	1.3E6 16 bit words	1.9E6

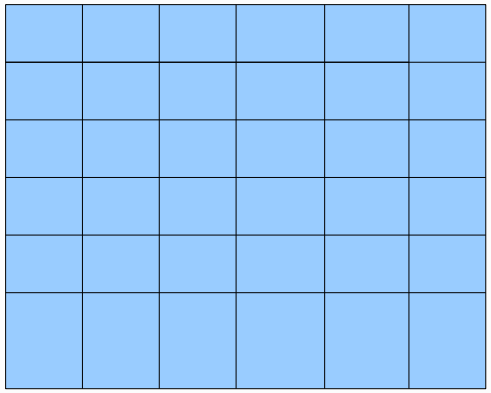
Word-aligned, 1ms spill, 12 AMC cards (60 channels) = 21E6 words (42E6 bytes)
If we allow 64MB per event we can store 8 events in the SDRAM

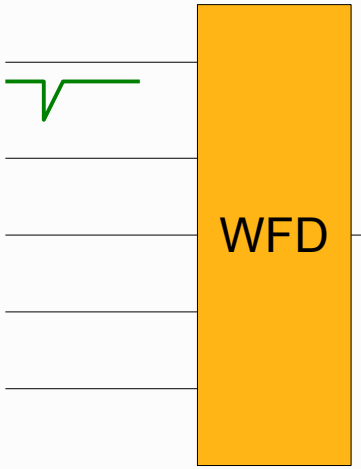
Proposed Firmware Tasks

- Increase AMC13 maximum payload sizes:
  - AMC payload to 4M words (8MB)
  - Per-calo event size to 64MB
    - This would allow for up to 1ms on 5 channels
- Modify AMC-AMC13 link to eliminate trigger features and associated overhead
  - Port AMC end of link to WFD board FPGA and provide as reference design
- Add “user processing” block on event builder output
  - For i.e. zero suppression, histogramming
- Add “link quiet” signal to suppress transfer during spill

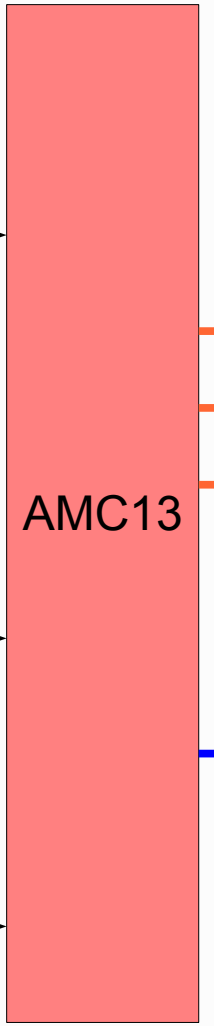
Reserve Slides

Calo (segmentation 9x6 or t.b.d.)

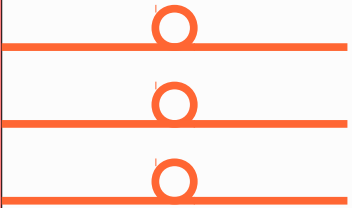




Backplane links
Currently: 2.5Gb/s
with 50% overhead
Can upgrade to 5Gb/s
with low overhead



3x 10Gb links
(protocol t.b.d)



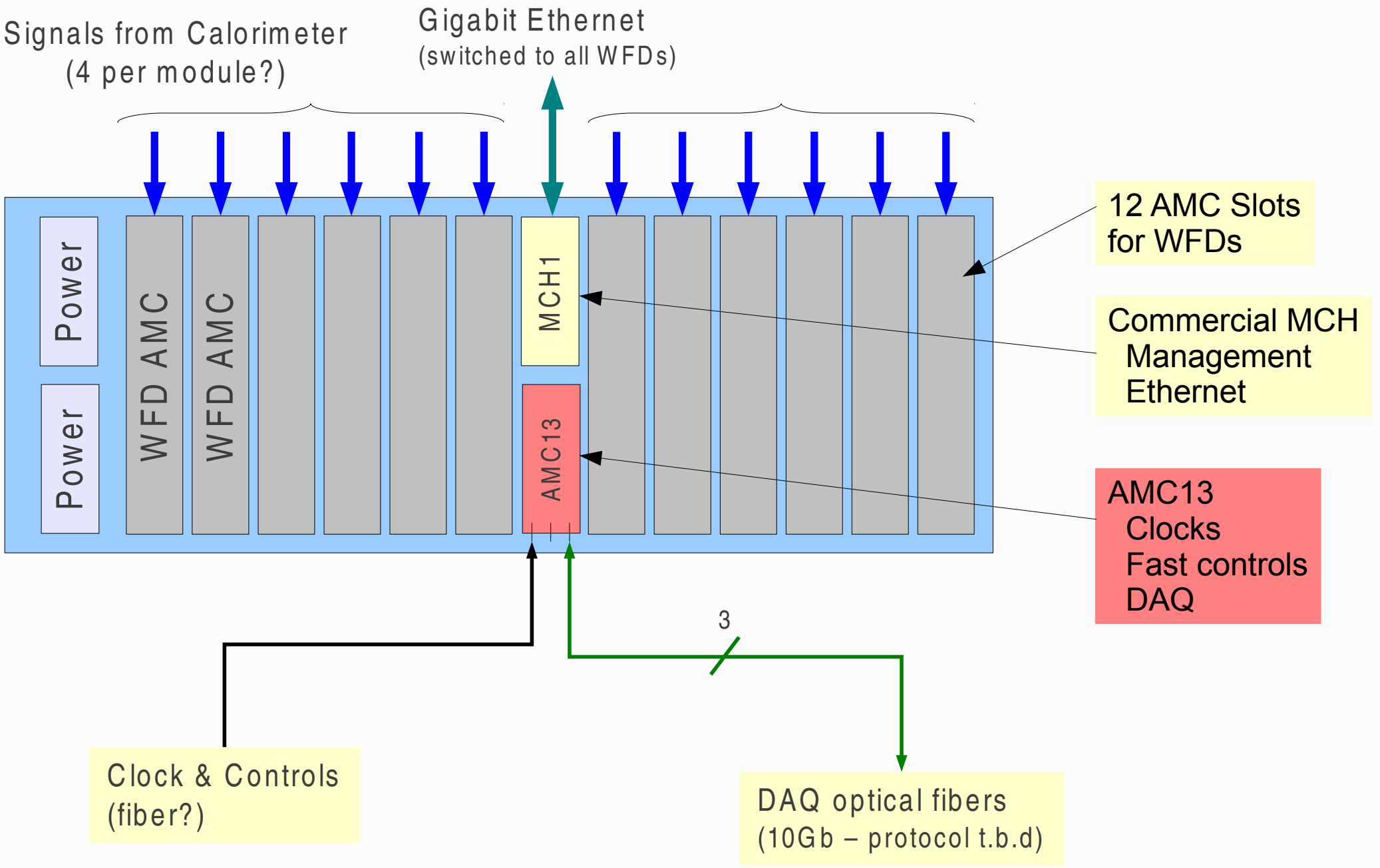
1 GbE via MCH

Rates per WFD module
5 ch * 12 bits at 500MS/s
Raw data rate during spill = 30Gb/s
Readout 700uS in 10ms = 2.1Gb/s
24 Hz spills average = 500Mb/s

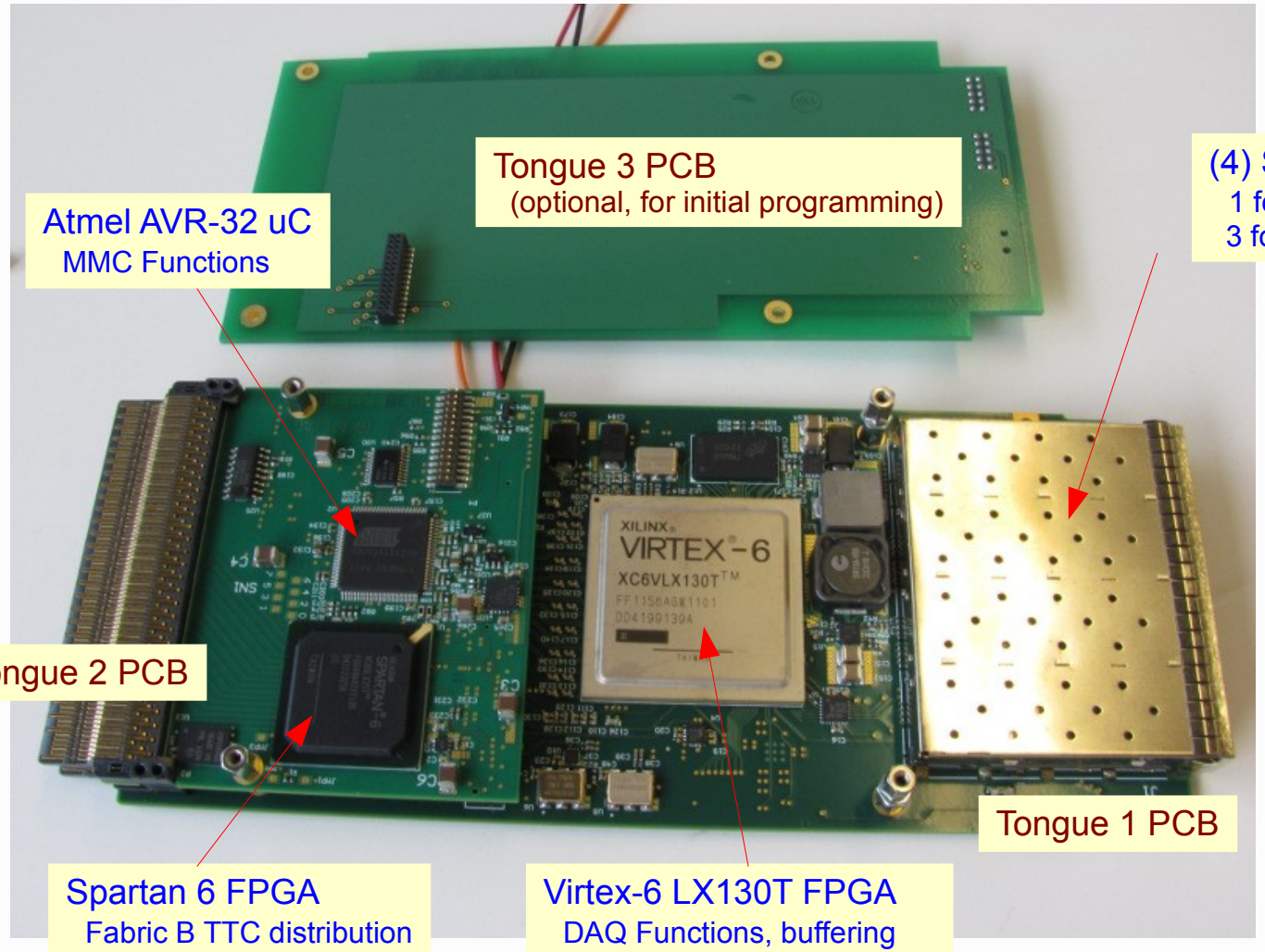
No zero suppression:
500MSPS * 700uS * 54 ch
* 12 bits * 24Hz = 5.5Gb/s average

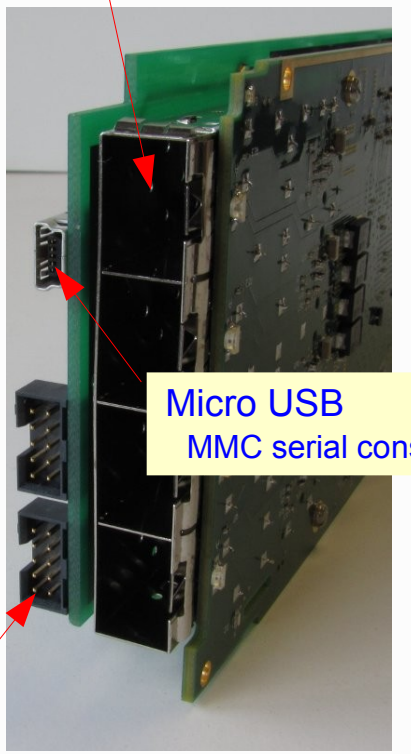
With zero suppression:
Would likely fit in GbE!

g-2 uTCA WFD Crate

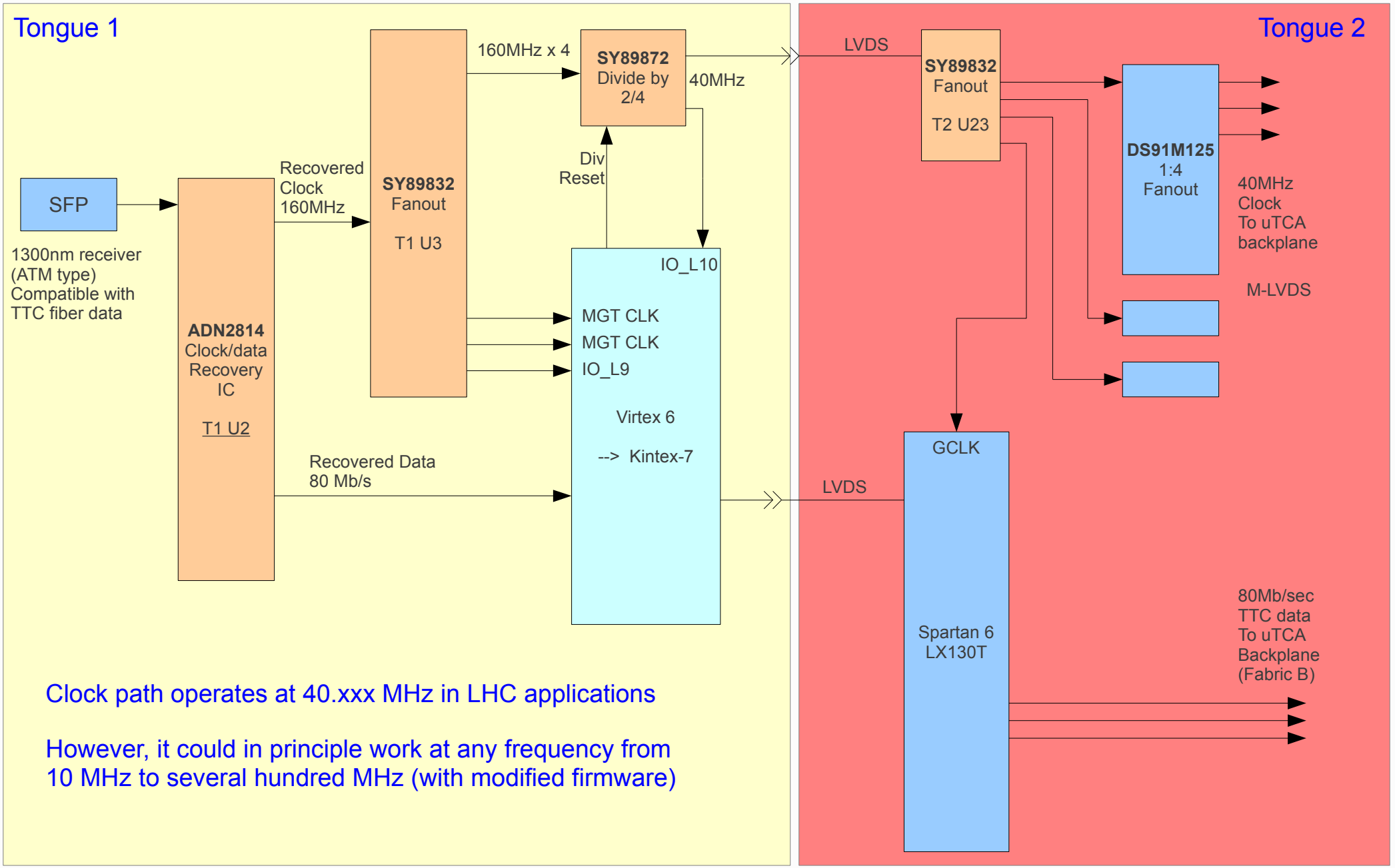


AMC13 Rev 1 Hardware





AMC13 Clocks



Clock path operates at 40.xxx MHz in LHC applications

However, it could in principle work at any frequency from 10 MHz to several hundred MHz (with modified firmware)